| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 1 | 418 | connectors and substrate and inductors and coupling | USPAT; US-PGPUB | 2003/11/07 15:16 |
| 2 | 63 | (connectors and substrate and inductors and coupling ) and receiver and driver | USPAT; US-PGPUB | 2003/11/07 15:04 |
| 3 | 38 | ((connectors and substrate and inductors and coupling ) and receiver and driver) and @ad<20011128 | USPAT; US-PGPUB | 2003/11/07 16:13 |
| 4 | 324 | (connectors and substrate and inductors and coupling ) and @ad<20011128 | USPAT; US-PGPUB | 2003/11/07 15:11 |
| 5 | 287 | ((connectors and substrate and inductors and coupling ) and @ad<20011128) and (array or plurality) | USPAT; US-PGPUB | 2003/11/07 15:12 |
| 6 | 33 | ((connectors and substrate and inductors and coupling ) and @ad<20011128) and (inductors with (array or plurality)) | USPAT; US-PGPUB | 2003/11/07 15:12 |
| 7 | 32 | (((connectors and substrate and inductors and coupling ) and @ad<20011128) and (inductors with (array or plurality))) not (((connectors and substrate and inductors and coupling ) and receiver and driver) and @ad<20011128) | USPAT; US-PGPUB | 2003/11/07 15:12 |
| 8 | 1 | connectors and substrate and inductors and coupling | EPO; JPO; DERWENT | 2003/11/07 15:16 |
| 9 | 6 | connectors and substrate and inductors | EPO; JPO; DERWENT | 2003/11/07 15:17 |
| 10 | 28 | connector and (array with inductors) and substrate | USPAT; US-PGPUB | 2003/11/07 16:21 |
| 11 | 23 | (connector and (array with inductors) and substrate) and @ad<20011128 | USPAT; US-PGPUB | 2003/11/07 16:18 |
| 12 | 56 | connector and (array with inductors) | USPAT; US-PGPUB | 2003/11/07 16:18 |
| 13 | 47 | (connector and (array with inductors) ) and @ad<20011128 | USPAT; US-PGPUB | 2003/11/07 16:20 |
| 14 | 24 | ((connector and (array with inductors) ) and @ad<20011128) not (connector and (array with inductors) and substrate) | USPAT; US-PGPUB | 2003/11/07 16:18 |
| 15 | 77 | connector and (plurality with inductors) and substrate | USPAT; US-PGPUB | 2003/11/07 16:20 |
| 16 | 227 | connector and (plurality with inductors) | USPAT; US-PGPUB | 2003/11/07 16:20 |
| 17 | 184 | (connector and (plurality with inductors) ) and @ad<20011128 | USPAT; US-PGPUB | 2003/11/07 17:28 |
| 18 | 184 | ((connector and (plurality with inductors) ) and @ad<20011128) not (((connectors and substrate and inductors and coupling ) and receiver and driver) and @ad<20011128) | USPAT; US-PGPUB | 2003/11/07 16:20 |
| 19 | 177 | (((connector and (plurality with inductors) ) and @ad<20011128) not (((connectors and substrate and inductors and coupling ) and receiver and driver) and @ad<20011128)) not (connector and (array with inductors) and substrate) | USPAT; US-PGPUB | 2003/11/07 16:21 |
| 20 | 174 | ((((connector and (plurality with inductors) ) and @ad<20011128) not (((connectors and substrate and inductors and coupling ) and receiver and driver) and @ad<20011128)) not (connector and (array with inductors) and substrate)) not (((connector and (array with inductors) ) and @ad<20011128) not (connector and (array with inductors) and substrate)) | USPAT; US-PGPUB | 2003/11/07 17:27 |
| 21 | 1385 | microelectronic and inductor | USPAT; US-PGPUB | 2003/11/07 17:28 |
| 22 | 113 | (microelectronic and inductor) and ((array or plurality) with inductors) | USPAT; US-PGPUB | 2003/11/07 17:34 |
| 23 | 92 | ((microelectronic and inductor) and ((array or plurality) with inductors)) and @ad<20011128 | USPAT; US-PGPUB | 2003/11/07 17:28 |

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|---|---|---|---|---|
| 24 | 84 | (((microelectronic and inductor) and ((array or plurality) with inductors)) and @ad<20011128) not (((((connector and (plurality with inductors) ) and @ad<20011128) not (((connectors and substrate and inductors and coupling ) and receiver and driver) and @ad<20011128)) not (connector and (array with inductors) and substrate)) not (((connector and (array with inductors) ) and @ad<20011128) not (connector and (array with inductors) and substrate))) | USPAT; US-PGPUB | 2003/11/07 17:29 |
| 25 | 82 | ((((microelectronic and inductor) and ((array or plurality) with inductors)) and @ad<20011128) not (((((connector and (plurality with inductors) ) and @ad<20011128) not (((connectors and substrate and inductors and coupling ) and receiver and driver) and @ad<20011128)) not (connector and (array with inductors) and substrate)) not (((connector and (array with inductors) ) and @ad<20011128) not (connector and (array with inductors) and substrate)))) not (connector and (array with inductors) and substrate) | USPAT; US-PGPUB | 2003/11/07 17:29 |
| 26 | 82 | (((((microelectronic and inductor) and ((array or plurality) with inductors)) and @ad<20011128) not (((((connector and (plurality with inductors) ) and @ad<20011128) not (((connectors and substrate and inductors and coupling ) and receiver and driver) and @ad<20011128)) not (connector and (array with inductors) and substrate)) not (((connector and (array with inductors) ) and @ad<20011128) not (connector and (array with inductors) and substrate)))) not (connector and (array with inductors) and substrate)) not (((connector and (array with inductors) ) and @ad<20011128) not (connector and (array with inductors) and substrate)) | USPAT; US-PGPUB | 2003/11/07 17:29 |
| 27 | 1 | (microelectronic and inductor) and (DC adj offset adj compensating adj receiver) | USPAT; US-PGPUB | 2003/11/07 17:35 |
| 28 | 1 | DC adj offset adj compensating adj receiver | USPAT; US-PGPUB | 2003/11/07 17:36 |
| 29 | 1 | offset adj compensating adj receiver | USPAT; US-PGPUB | 2003/11/07 17:36 |
| 30 | 47 | compensating adj receiver | USPAT; US-PGPUB | 2003/11/07 17:36 |
| 31 | 20 | (compensating adj receiver) and DC | USPAT; US-PGPUB | 2003/11/07 17:36 |
| 33 | 0 | ((compensating adj receiver) same DC) and (mode adj drive) | USPAT; US-PGPUB | 2003/11/07 17:37 |
| 34 | 0 | ((compensating adj receiver) same DC) and (current adj drive) | USPAT; US-PGPUB | 2003/11/07 17:37 |
| 35 | 1 | ((compensating adj receiver) same DC) and driver | USPAT; US-PGPUB | 2003/11/07 17:37 |
| 32 | 3 | (compensating adj receiver) same DC | USPAT; US-PGPUB | 2003/11/07 17:38 |

US-PAT-NO: 6529385

DOCUMENT-IDENTIFIER: US 6529385 B1

TITLE: Component array adapter

DATE-ISSUED: March 4, 2003

US-CL-CURRENT: 361/766, 361/735 , 361/736 , 361/760 , 361/761 , 361/763
, 361/764 , 361/782 , 361/785 , 361/803 , 361/811

APPL-NO: 09/ 382348

DATE FILED: August 25, 1999

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Application Filing Date - AD (1):
**19990825**

Brief Summary Text - BSTX (12):
Another embodiment includes a method for testing an integrated circuit. The method includes connecting at least one test probe to an adapter. The adapter includes an insulating substrate having first and second sides and a plurality of sites. Each site includes a first node on the first side, a second node on the second side and at least one component connected between the first and second nodes. The components include active or passive components. Each component is substantially normal to the first and second sides of the insulating substrate. Each site further includes a first electrical **connector** connected to the second node. The method further includes connecting the adapter to the integrated circuit using the first

electrical connectors of the
plurality of sites and testing the integrated circuit using a test unit
attached to each of the test probes.

Detailed Description Text - DETX (17):
FIG. 2A illustrates a top view of one embodiment of an interconnect system
200. For one embodiment, electrical connectors 222 are connected to the top
side 230 of the insulating substrate 220. For one embodiment, the electrical
connectors are standard socket pins similar to those found on a standard Ball
Grid Array (BGA) socket. BGA adapters are well known in the art and are not
detailed here. Each electrical **connector** 222 is connected to a node 226 on the
top side 230 of the insulating substrate 220 to provide a point for other
devices to connect to the components in the insulating substrate 220. For
another embodiment, a standard BGA socket is connected to the top side 230 of
the insulating substrate 220 using the electrical contacts, often standard BGA
solder balls, attached on the bottom side of the BGA socket. The electrical
contacts are connected to each node 226 on the top side 230 of the insulating
substrate 220. The electrical connectors, often socket pins, on the top side
of the BGA socket perform the same function as the electrical connectors 222
described above.

Detailed Description Text - DETX (19):
FIG. 3 is a side view of one embodiment of a circuit board interface system
300. For one embodiment, the circuit board interface system 300 has a circuit
board 360, an interconnect device 100 and a BGA socket 310. For one
embodiment, the circuit board 360 is a mother board of a personal computer or
other processor-based system. The circuit board 360 has a

number of signal
paths (not shown) that carry signals. For one embodiment the signal paths are
from a microprocessor bus. For another embodiment, the signal paths are from a
memory data bus. The interconnect device 100 is connected to the circuit board
360 using electrical connectors 324. In one embodiment, as shown in FIG. 3,
electrical connectors 324 are solder balls. In general, electrical connectors
324 can be any conductive material known to those of skill in the art. Each
electrical **connector** 324 connects a node 326 on the bottom side 340 of the
interconnect device 100 to one or more of the signal paths on the circuit board
360.The interconnect device includes the structure described above in
conjunction with FIGS. 1A and 1B. The interconnect device 100 is connected to
the BGA socket 310 using electrical contacts 314, usually standard solder ball
connectors, on the BGA socket 310. For another embodiment, the BGA socket 310
is replaced by electrical connectors integrated onto the interconnect device
100. For one embodiment, the electrical connectors are similar to the standard
socket pins on a BGA socket and perform substantially the same function. For
another embodiment, the circuit board interface system 300 has alignment pins
302 used to align the BGA socket 310, the interconnect device 100 and the
circuit board 360.

Detailed Description Text - DETX (21):

For one embodiment, shown in FIG. 4, the instrumentation probe 470 is
connected to the BGA socket 410 using the pins 472. Each pin 472 is connected
to an electrical **connector** 412, typically a standard socket, on the BGA socket
410. The BGA socket 410 is connected to the interconnect device 100 by
connecting the electrical contacts 414, usually standard

solder ball
connectors, on the BGA socket 410 to the nodes 426 on the top side 430 of the
interconnect device 100. For another embodiment, the BGA socket 410 is
replaced by electrical connectors integrated onto the top side 430 of the
interconnect device 100 at each node 426. For one embodiment, the electrical
connectors are similar to the standard socket pins on a BGA socket and perform
substantially the same function. For another embodiment, the test device 400
has alignment pins 402 used to align the BGA socket 410 and the interconnect
device 100.

Claims Text - CLTX (2):
2. The interconnect device of claim 1, wherein the **plurality** of active or
passive electrical components are selected from the group comprising resistors,
capacitors, **inductors** and diodes.

Claims Text - CLTX (8):
8. The test device of claim 7 where the **plurality** of active or passive
electrical components are selected from the group comprising resistors,
capacitors, **inductors** and diodes.

Claims Text - CLTX (14):
14. The method of claim 12 where the **plurality** of active or passive
electrical components are selected from the group comprising resistors,
capacitors, **inductors** and diodes.

Claims Text - CLTX (19):
19. The interface system of claim 18, wherein the **plurality** of active or
passive electrical components are selected from the group comprising resistors,
capacitors, **inductors** and diodes.

Claims Text - CLTX (32):

32. The interconnect device of claim 29 where at least one of the **connector** is offset.